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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,234	09/08/2003	Youngoo Yang	0140115	4107

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,234	YANG ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10 and 17* is/are rejected.

7)☒ Claim(s) *11-15 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Jan 6, 2005 was reviewed and considered with the following results:

The new abstract overcame its objections described in the previous Office Action, and those objections have now been withdrawn.

The changes to the specification overcame the various objections to the disclosure, which have also been withdrawn.

The cancellation of claims 9 and 16 rendered their respective objections and rejections moot.

After reconsidering the active claims, an inadvertent oversight (e.g. it wasn't described in the previous Office Action) in claim 15 was noted. This is described later under the Claim Objections.

Amended claims 1, 8, and 15 overcame the rejections of claims 1-8, 10-15, and 17-20 under 35 U.S.C. 112 as described in the previous Office Action. Therefore, those rejections have been withdrawn. However, the cancellation of claims 9 and 16 created new rejections with respect to claims 10 and 17, which are described later under the appropriate section.

Amended claim 1, and its associated comments on page 14 of the amendment, overcame the rejections of claims 1, and 3-7 under 35 U.S.C. 103(a) with respect to Finlay et al. The Finlay reference is assigned to Skyworks Solutions, Inc., the same assignee as the present application. [Note: Due to mergers, Skyworks Solutions, Inc. is also related to Conexant Systems, Inc. and Alpha Industries, Inc.] Although those previous Office Action's prior art

rejections have now been withdrawn, the examiner has now rejected those claims under 35 U.S.C. 103(a) using other prior art, and has also made double patenting rejections after another related application was found during the update search. These new rejections are described later under the appropriate section. Therefore, this action is NON-FINAL.

Claim Objections

Claims 15, and 17-20 are objected to because of the following informality: Clam 15, line 18 should have --and-- added after "voltage;" to clearly indicate the "fifth resistor" section is the last limitation to be cited within the claim. Claims 17-20 carry over the objection from claim 15. An appropriate correction is required.

Claim Rejections - 35 USC § 112

Claims 10 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. Both claims now depend on a cancelled claim. Therefore, it is suggested their dependency be changed to indicate the independent claim upon which they depend.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

At least claims 1-8, and 10 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over related claims 1, 4-5, 8-11, 14, and 16-18 of copending Application No. 10/637,146 (found under US 2005/0030105 A1, published Feb 10, 2005, during the recent update search). Although the conflicting claims are not identical, they are not patentably distinct from each other because it is obvious the basic difference(s) between the present application's claims, and those within 10/637,146, is how the limitations are recited, and the present invention's independent claim 8 includes an extra resistor (i.e. a third resistor) not recited within any of the other application's claims. For example, the bias control circuit, bias circuit, amplifier transistor, first-third bias transistors, base connections of the first and second bias transistors with the third bias transistor's collector, first node, and means of the present application's claim 1 correspond to the control circuit, bias circuit, amplifier's fourth bipolar transistor, first-third bipolar transistors, first node, second node, and control circuit, respectively recited within claim 1 of application 10/637,146. Although the present application's claim 1 cites a bias control circuit the comprises means for receiving a control voltage, and means for actively adjusting an equivalent resistance, one of ordinary skill in the art would obviously understand these means correspond to the fifth bipolar transistor/second-fourth resistors and the control voltage of the control circuit of application 10/637,146's dependent claim 5. Those means of claim 1 also correspond to the fifth bipolar transistor/second-fourth resistors and the control voltage recited within application 10/637,146's independent claim 8, as well as within dependent claim 18. Other than some obvious labeling differences, the

recited elements (with the exception of a "third resistor connected across said emitter of the bias control transistor and said first reference voltage") within claim 8 of the present application are recited within various claims within application 10/637,146. For example, the bias control transistor, and the first, second, and fourth resistors, of the present application's independent claim 8's bias control circuit correspond to the fifth bipolar transistor, and the second-fourth resistors, respectively within the control circuit of application 10/637,146's dependent claim 5, independent claim 8, and dependent claim 18. However, instead of having a (third) resistor connected across the emitter of the bias control transistor and the first reference voltage as recited within the present application's claim 8, the other application's claims have the emitter of the fifth bipolar transistor (e.g. the bias control transistor) coupled to ground (e.g. the first reference voltage). [Note: No direct connection between the emitter and ground is cited.] Therefore, it would have been obvious to one of ordinary skill in the art that application 10/637,146 could have disclosed, shown, and claimed that a resistor could be added between the fifth bipolar transistor and ground. That resistor would provide another voltage drop across the second resistor and fifth bipolar transistor when the transistor is conducting, thus effectively changing the equivalent resistance (and voltage drop) between the first node and the first reference voltage. The fifth resistor and the second reference voltage of the present application's claim 11, which depends on claim 8, corresponds to the first resistor and reference voltage recited within application 10/637,146's claims 1, 8 and 14. Since the basic structure of the present application's bias control circuit (e.g. see claims 1, 8 and 14; and "106" of the applicant's Fig. 1) is understood to correspond to the control circuit of application 10/637,146's claims 1, 5, 8, and 18 (e.g. see "212" of that application's Fig. 2)), it would be obvious to one of ordinary

skill in the art that the circuits recited within application 10/637,146 would also provide the same type of functions (e.g. decreasing resistance, increasing current of the (bias) control circuit, and/or increasing the (amplifier) fourth transistor's quiescent current) when the control voltage is increased. Also, is also noted that some of application 10/637,146's claims (e.g. see claims 3-4 and 9-11) recite limitations related to increased/reduced current and/or increased/reduced resistance that one of ordinary skill in the art would understand correspond to the present application's limitations recited within claims 2-4. Also, since application 10/637,146 discloses the relationships of the circuitry/transistors to a "die area" (e.g. see paragraphs 0005, 0008, 0023, and 0025), and the invention is related to high-power amplifiers, it would be obvious to one of ordinary skill in the art that the claims of that application could have also indicated the circuits and transistors are integrated into a single die as recited within the present application's claim 5, and the (amplifier) fourth transistor could be a high-power CDMA transistor as recited within the present application's claim 6.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyazawa, a reference found during a recent update search.).] Fig. 2 shows bias control circuit 29; bias circuit 22-27 with first-third bias transistors 24,22,23; and amplifier transistor 21. Since the structural relationships of 24,22,23,21,27,29 of Miyazawa's Fig. 2 correspond to 114,116,118, 110,120,106, respectively of the applicants' own Fig. 1, it is not necessary to describe all the connections and nodes. The basic difference is with respect to Miyazawa's bias control circuit 29 coupled to the first node (the base of third bias transistor 23 and emitter of first bias transistor 24) versus the applicants' bias control circuit 106 coupled to first node 126. Miyazawa's bias control circuit 29 does not have a means for receiving a control voltage, nor a means for actively adjusting an equivalent resistance between the first node and a reference voltage (e.g. ground). It would have been obvious to one of ordinary skill in the art to replace bias control circuit (resistor) 29 of Miyazawa with at least one (bipolar) transistor receiving a control voltage to effectively function as a variable resistance within the circuit. When bias control circuit 29 is replaced by a (bipolar) transistor and its control voltage (known means for providing a controlled, variable type resistance), the base of the transistor will be the means for receiving the control voltage, and the transistor itself will be the means for actively adjusting the equivalent

resistance between the first node and the reference voltage. Therefore, claim 1 is rendered obvious. With resistor 29 circuit replaced by at least one transistor, the quiescent current and desired output level can be adjusted to meet the requirements of the circuitry it will be associated with. Also, the transistor(s) will take up less area than a discrete resistor. When bias control circuit 29 is replaced by an NPN transistor (e.g. to correspond to the other NPN transistors within the circuit), its equivalent resistance will decrease when the control voltage increases (i.e. as the control voltage increases, the transistor's conductance increases along with the current drawn by the bias control circuit , thus decreasing the transistor's equivalent resistance). This renders obvious claims 2 and 3. Under these circumstances (i.e. an increase in control voltage), the voltage at the base of 23 will decrease, causing the voltages at the bases of 24 and 22 to increase and allowing 22 to conduct more. This will increase the base voltage of amplifier transistor 21, and it will also conduct more, thus its quiescent current will increase, and claim 4 is rendered obvious. It would have been obvious to one of ordinary skill to integrate the bias control circuit, bias circuit, and amplifier transistor into a single die, rendering obvious claim 5. The use of a single die would help minimize area, and also help ensure all the elements operate under substantially the same conditions (e.g. temperature). Miyazawa discloses the invention relates to a high frequency power amplifier carrying out power control of a CDMA system (e.g. see column 1, lines 8-16). Therefore it would have been obvious to one of ordinary skill in the art that amplifier transistor 21 can be a high-power CDMA transistor, rendering claim 6 obvious. Since the reference voltage (not labeled) is ground, claim 7 is rendered obvious. [Note: Although Fig. 5 of Miyazawa shows bias control circuit 31-34, the active adjusting of an equivalent resistance between the first node and the reference voltage is not clear because the diode

connected transistor 33 of current mirror 33,34 will allow the current through 34 to be changed, but the voltage drop across 33 will maintain a constant base voltage on 34, thus its resistance will probably not change.]

Claims 1-7 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (Yamamoto), another reference found during a recent update search.).] Fig. 2 shows bias control circuit R3; bias circuit R1,R4-R5,Tr1-Tr3 with first-third bias transistors Tr3,Tr1,Tr2; and amplifier transistor TrA. Since the structural relationships of Tr3,Tr1,Tr2,TrA, R1R3,R5 of Yamamoto's Fig. 2 correspond to 114,116,118,110,120,106,122 respectively of the applicants' own Fig. 1, it is not necessary to describe all the connections and nodes. The basic difference is with respect to Yamamoto's bias control circuit R3 coupled to the first node (the base of third bias transistor Tr2 and emitter of first bias transistor Tr3) versus the applicants' bias control circuit 106 coupled to first node 126. Yamamoto bias control circuit R3 does not have a means for receiving a control voltage, nor a means for actively adjusting an equivalent resistance between the first node and a reference voltage (e.g. ground). It would have been obvious to one of ordinary skill in the art to replace bias control circuit (resistor) R3 of Yamamoto with at least one (bipolar) transistor receiving a control voltage to effectively function as a variable resistance within the circuit. When bias control circuit R3 is replaced by a (bipolar) transistor and its control voltage, the base of the transistor will be the means for receiving the control voltage, and the transistor itself will be the means for actively adjusting the equivalent resistance between the first node and the reference voltage. Therefore, claim 1 is rendered obvious. With resistor R3 circuit replaced by at least one transistor, the quiescent current and desired output level can be adjusted to meet the requirements of the circuitry it will be associated with. Also, the

transistor(s) will take up less area than a discrete resistor. When bias control circuit R3 is replaced by an NPN transistor (e.g. to correspond to the other NPN transistors within the circuit), its equivalent resistance will decrease when the control voltage increases (i.e. as the control voltage increases, the transistor's conductance increases along with the current drawn by the bias control circuit , thus decreasing the transistor's equivalent resistance). This renders obvious claims 2 and 3. Under these circumstances (i.e. an increase in control voltage), the voltage at the base of Tr2 will decrease, causing the voltages at the bases of Tr3 and Tr1 to increase and allowing Tr1 to conduct more. This will increase the base voltage of amplifier transistor TrA, and it will also conduct more, thus its quiescent current will increase, and claim 4 is rendered obvious. It would have been obvious to one of ordinary skill to integrate the bias control circuit, bias circuit, and amplifier transistor into a single die, rendering obvious claim 5. For example, see column 2, lines 25-26). The use of a single die would help minimize area, and also help ensure all the elements operate under substantially the same conditions (e.g. temperature). Yamamoto discloses the invention relates to a power amplifier (e.g. see column 1, line 7). Therefore it would have been obvious to one of ordinary skill in the art that amplifier transistor TrA can be a high-power CDMA transistor, rendering claim 6 obvious. Since the reference voltage (not labeled) is ground, claim 7 is rendered obvious.

Claims 9 and 16 have been cancelled.

Allowable Subject Matter

Claims 11-15, and 18-20 are only objected to because: 1) claims 11-14 depend on rejected claim 8, and 2) of the previously described objection of independent claim 15. There is no motivation to modify or combine any prior art reference to ensure the bias control circuit also

comprises: 1) the sixth resistor as recited within claim 11; 2) the temperature compensation circuit as recited within claims 12 (upon which claim 13 depends) and 14; and 3) the bias control transistor, as well as the first-fifth resistors as recited within claim 15, upon which claims 18-20 depend.

Claim 17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. For example, if this claim was made to depend on independent claim 15, its dependency on a cancelled claim would be overcome.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Terry L. Englund
23 March 2005

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